Nanotechnology for High-Performance Computing

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Novel Device Group

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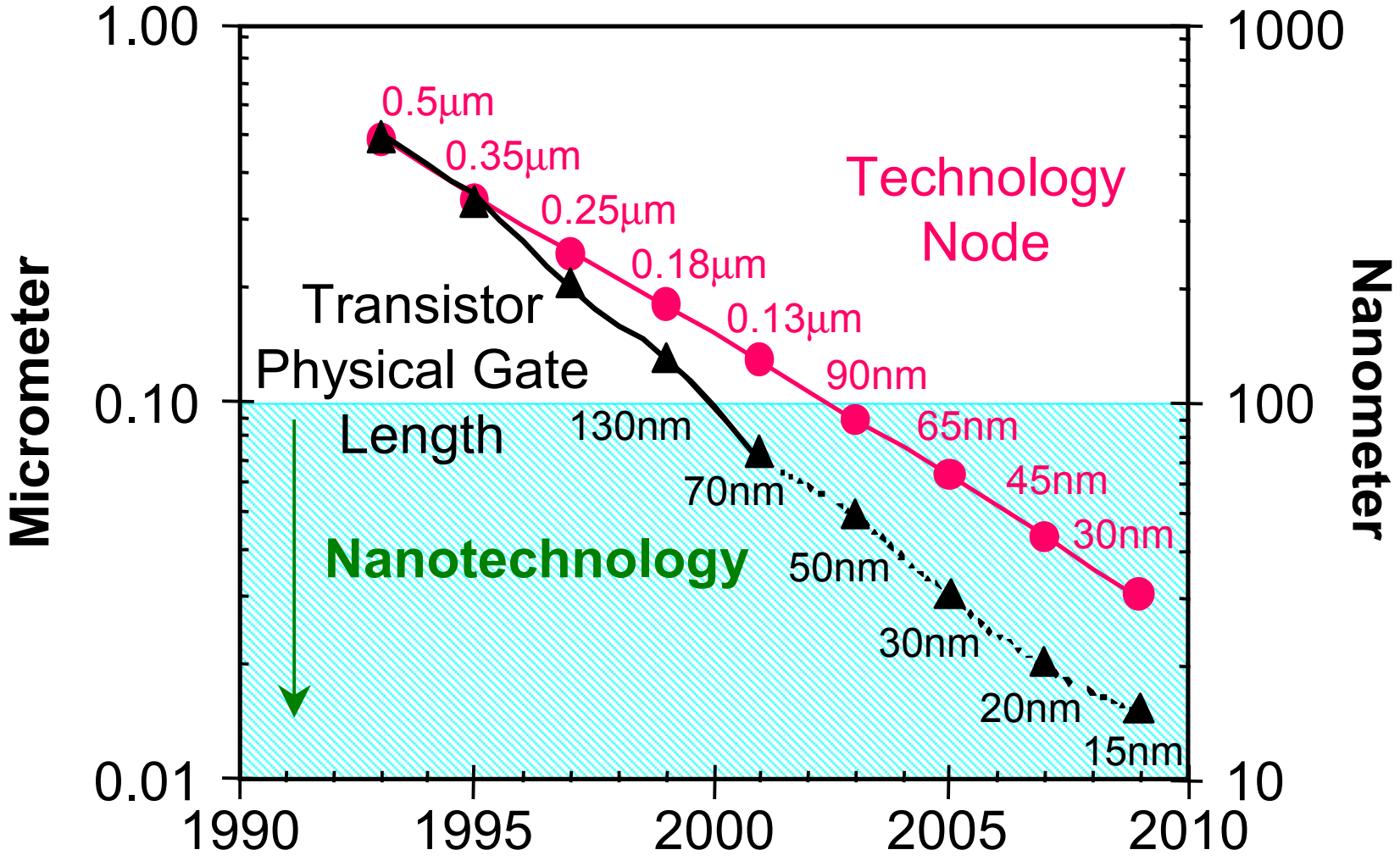
DARPA Workshop on the Integration of Scalable CMOS Systems with Novel Nanostructures

Content

- **Transistor scaling and Moore's law**
- **Silicon nano-transistors and new device architecture**
- **Examples of Silicon nano-technology and integration with novel nanostructures.**
- **Summary**

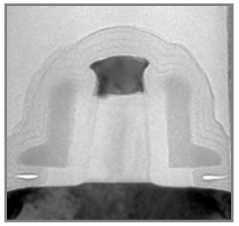
Moore's Law Continues…



Transistor physical gate length will reach ~15nm before end of this decade, and ~10nm early next decade

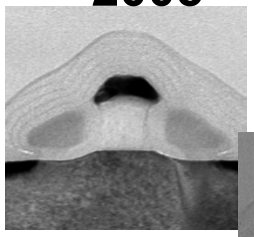
Silicon Transistor Scaling and Moore's Law will Continue through 2015 ……

90nm Node
2003



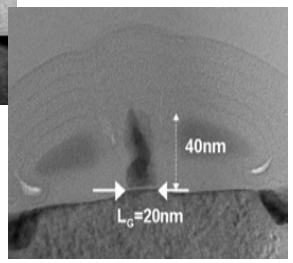
50nm Length

65nm Node
P1264
2005



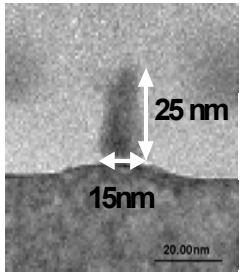
30nm
Prototype

45nm Node
P1266
2007



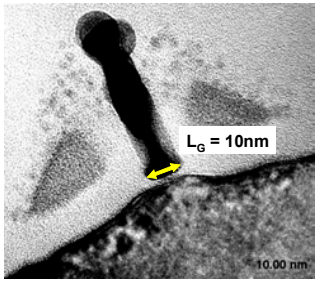
20nm Prototype

32nm Node
2009



15nm Prototype

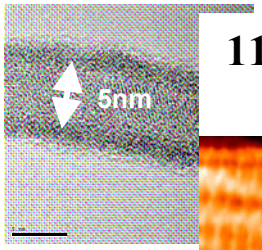
22nm Node
2011



10nm Prototype

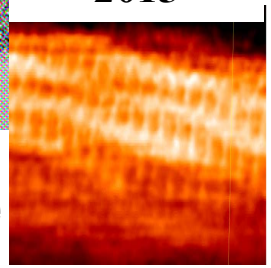
New materials integrated onto Si

16 nm node
2013



7nm
Si-Nanowire
Prototype

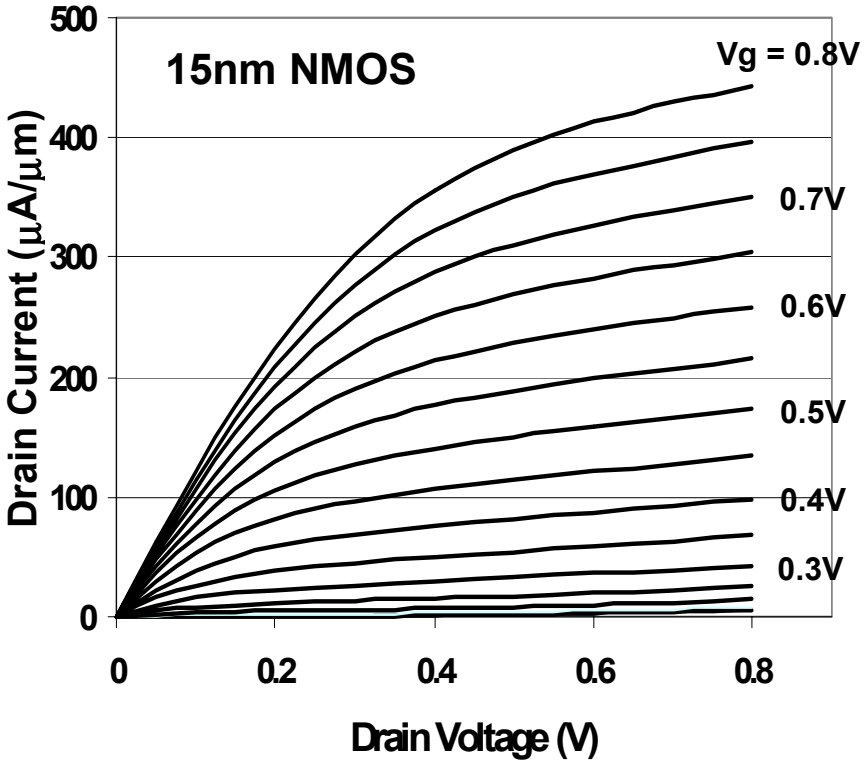
11nm node
2015

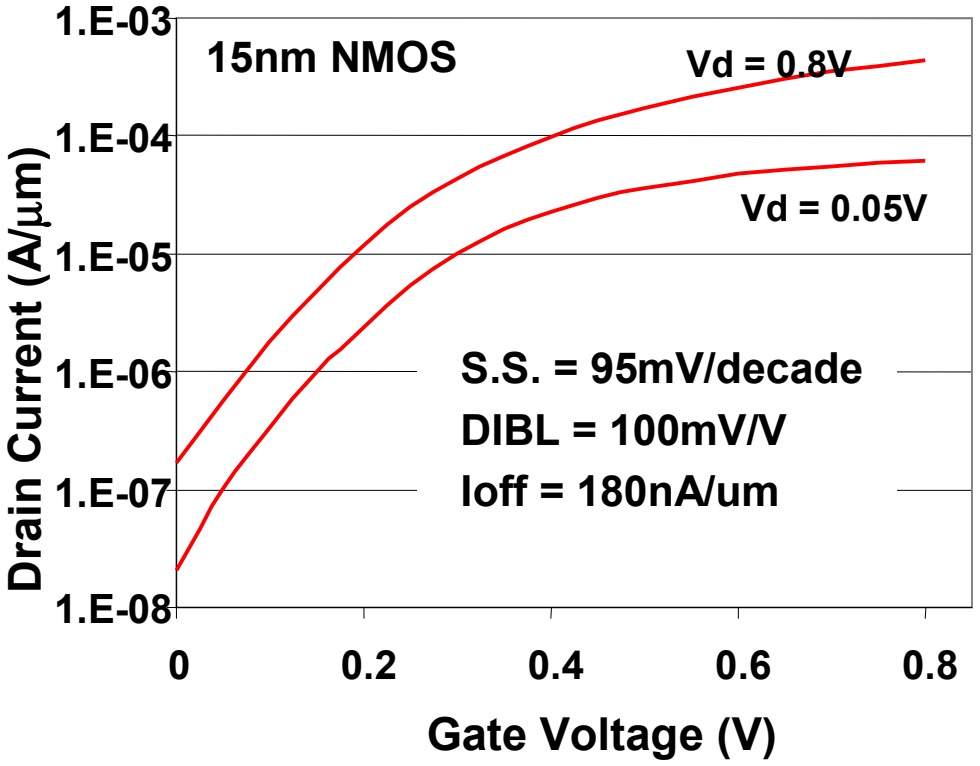


5nm
C-nanotube
Prototype

New electronic materials, nano-technologies and nano-architecture introduced along the way

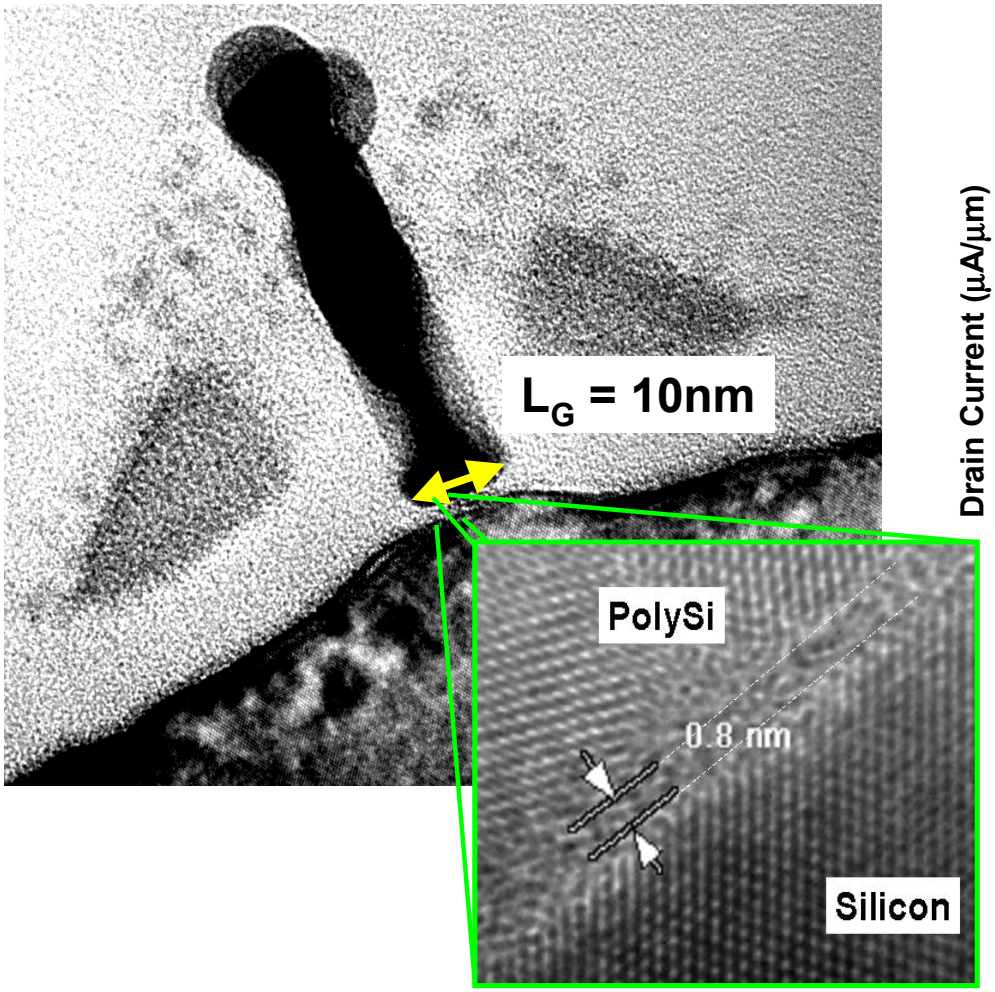
Experimental 15nm Si Transistor

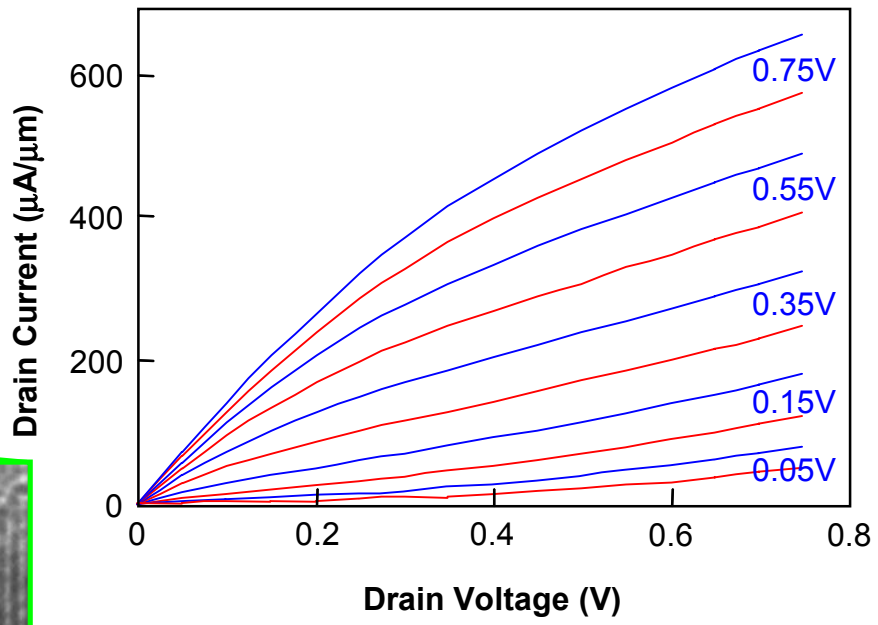




- **Well-controlled short channel characteristics**

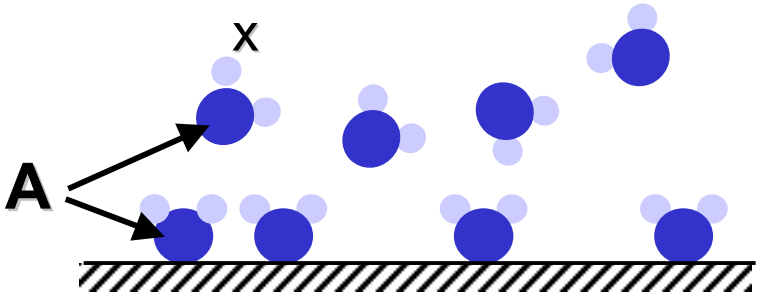
Experimental 10nm Si MOS Transistor



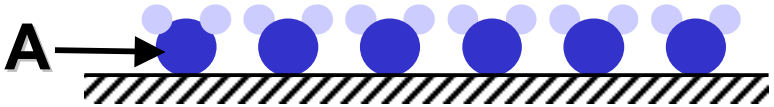


- **10nm transistor still behaves like a transistor!** Sort of…

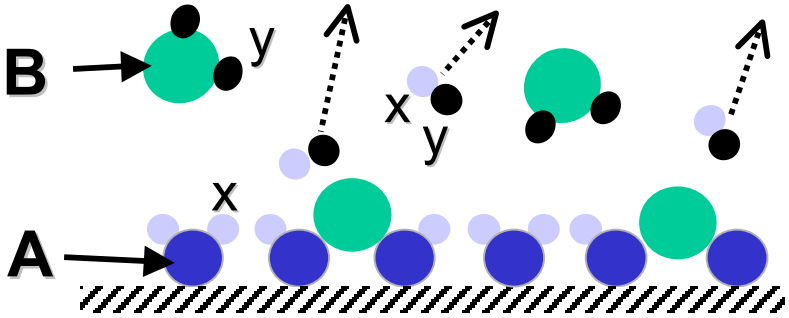
Nanotechnology Example: Crafting Thin Films with Atomic Layer Deposition (ALD)



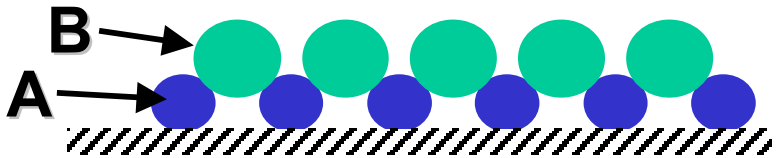
Step 1



Step 2



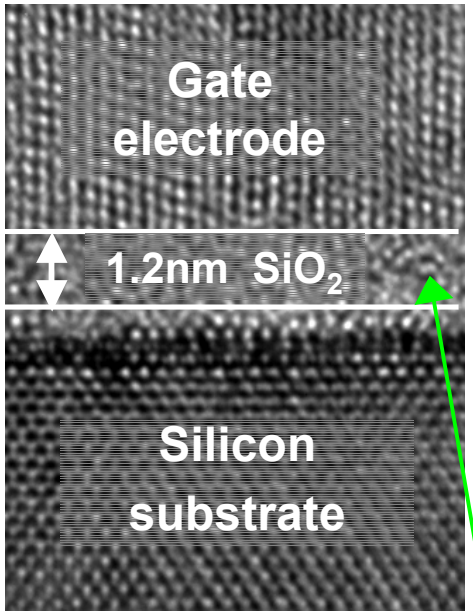
Step 3

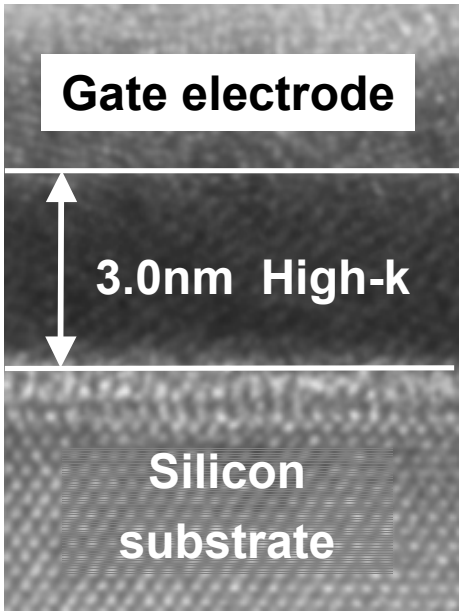


Step 4

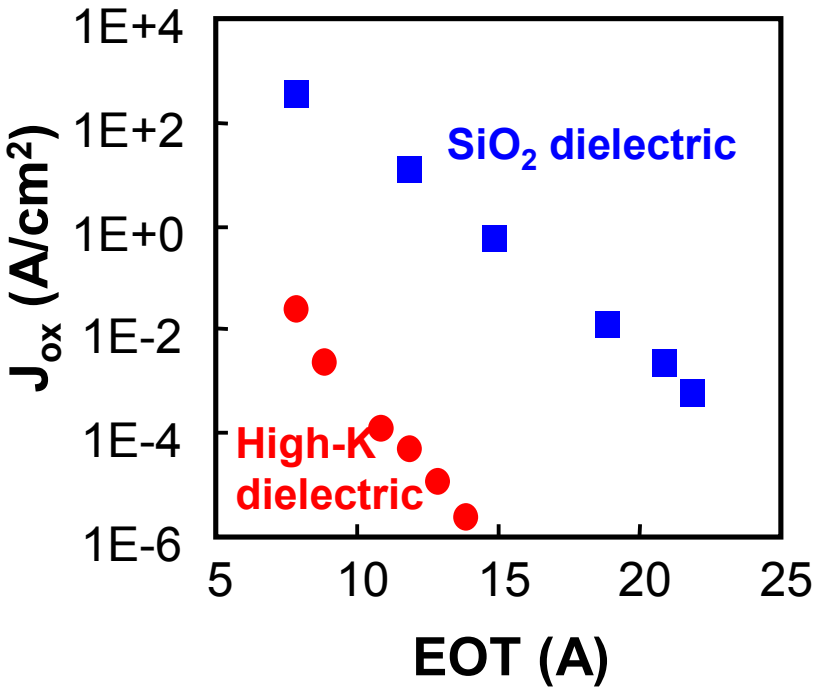
ALD: Today's nanotechnology for self-assembly by atomic layer

New Nanotechnology (e.g. ALD) to Craft New Material (e.g. High-K Gate Dielectrics)



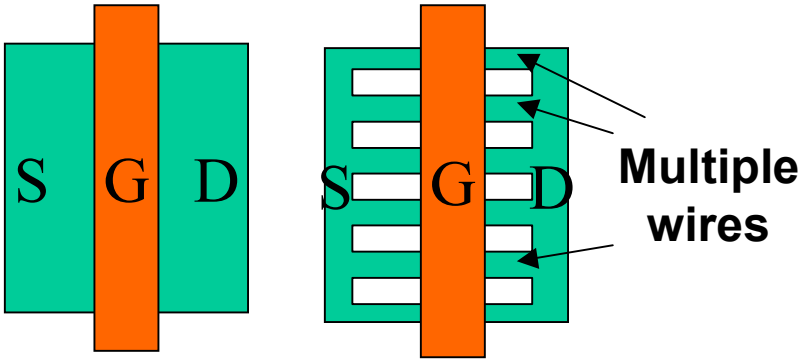


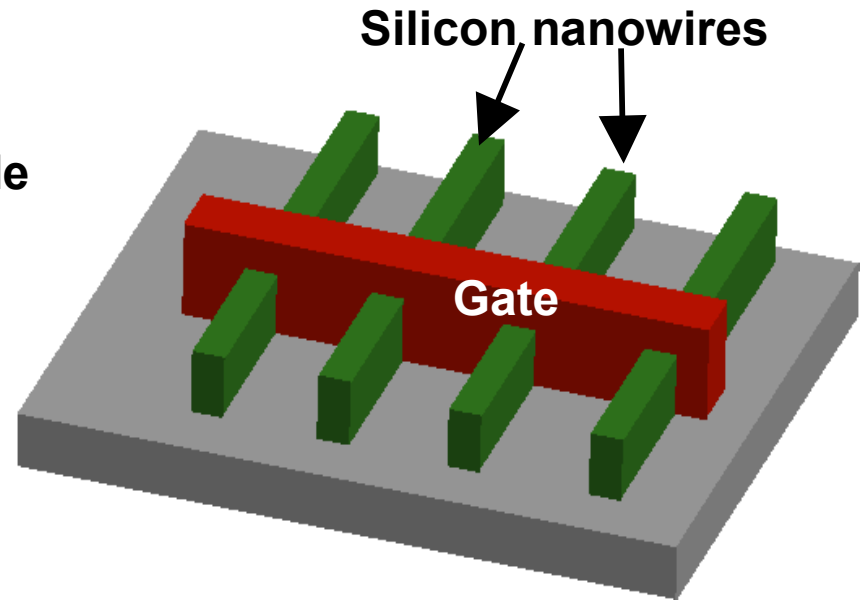
90 nm node (in production)



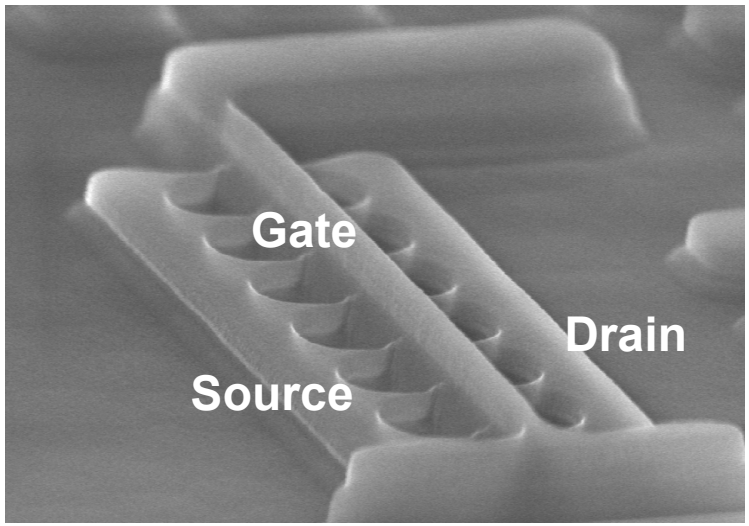
	SiO2	High-k
Capacitance:	1.0x	1.6x
Leakage:	1.0x	< 0.01x

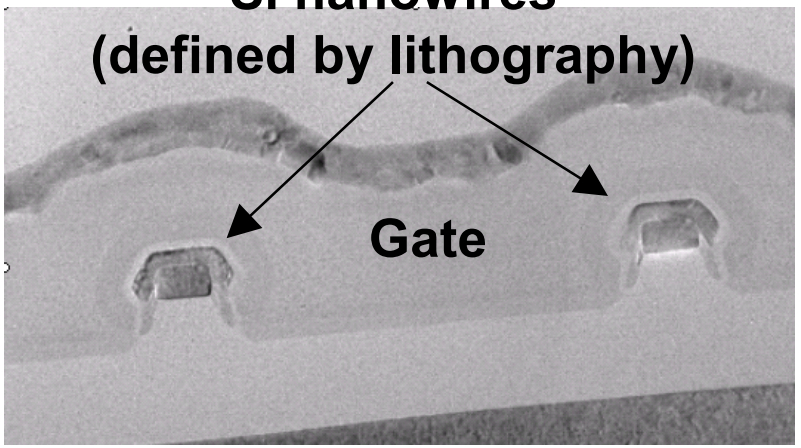
Nano-device Architecture





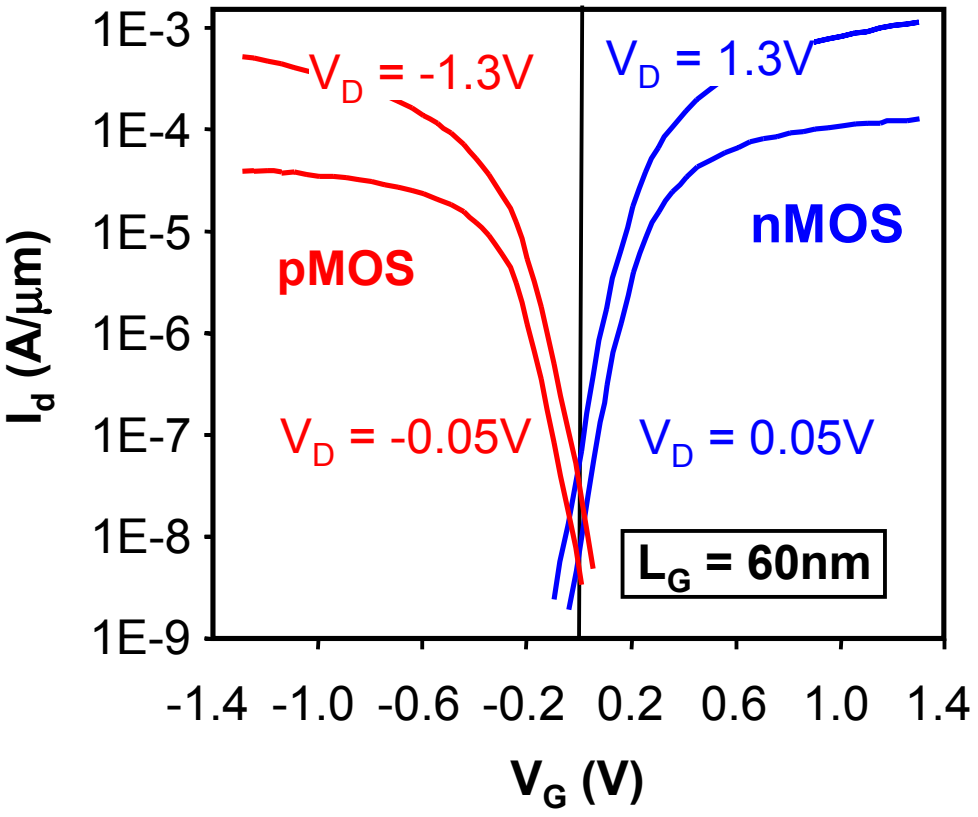
Total Drive Current =
I_d per nanotube/nanowire x no. of tubes/wires



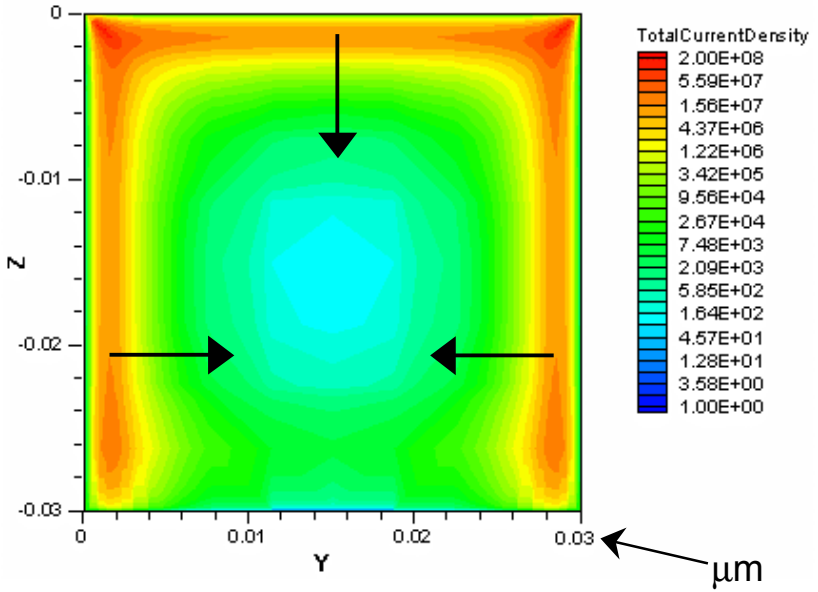


Si nanowire transistor in action:

$L_G = T_{Si} = W_{Si}$ for optimum performance



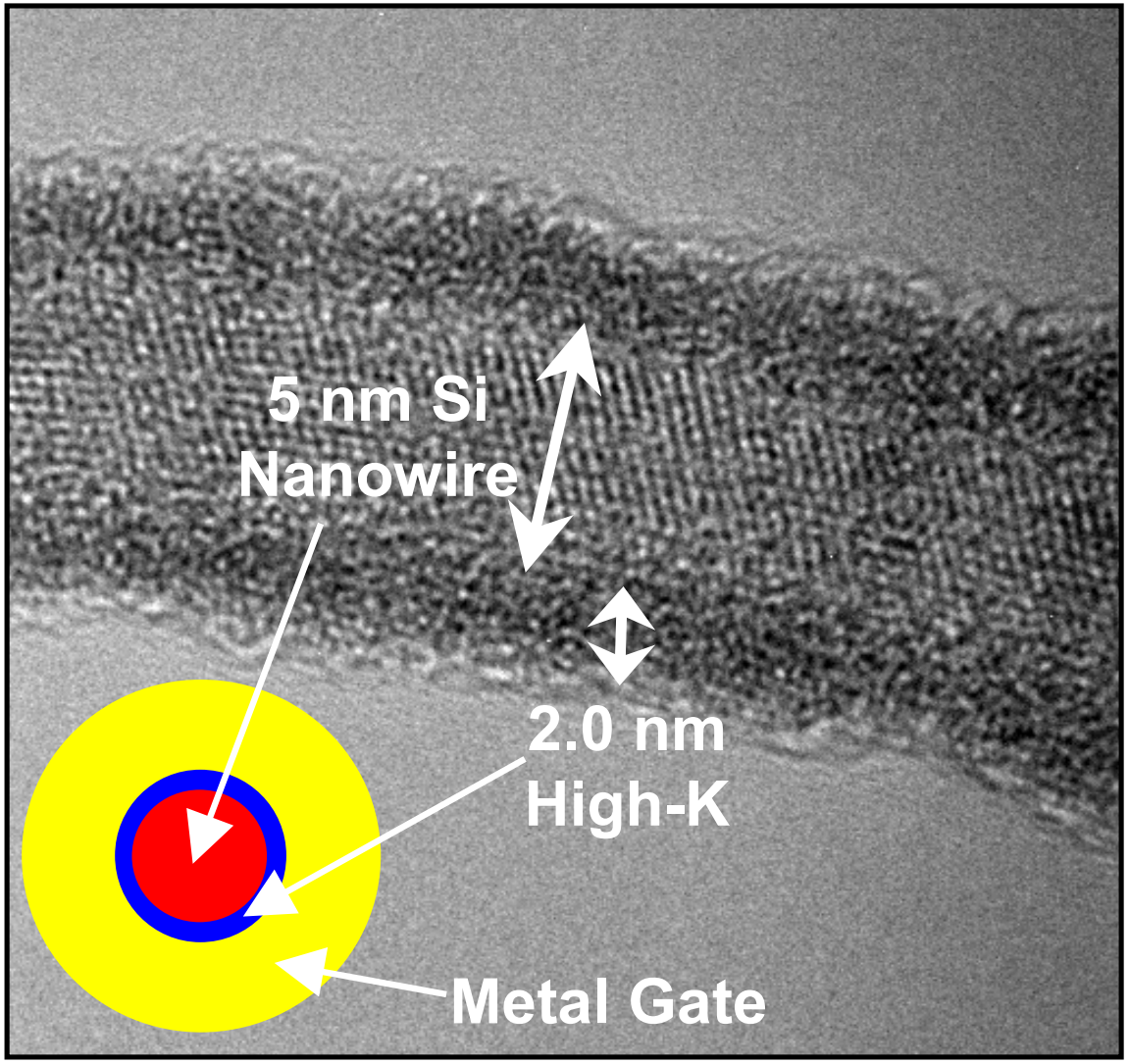
Simulation of the current density through the device:



Device scaling below ~10nm leaves only "inversion" layer in place

- **Better current density, better control of SCE, better off-state**

Nanotechnology Beyond 10nm Size (Beyond ~2013)



$L_G = T_{Si} = W_{Si}$
Decrease in L_G implies decrease in wire diameter

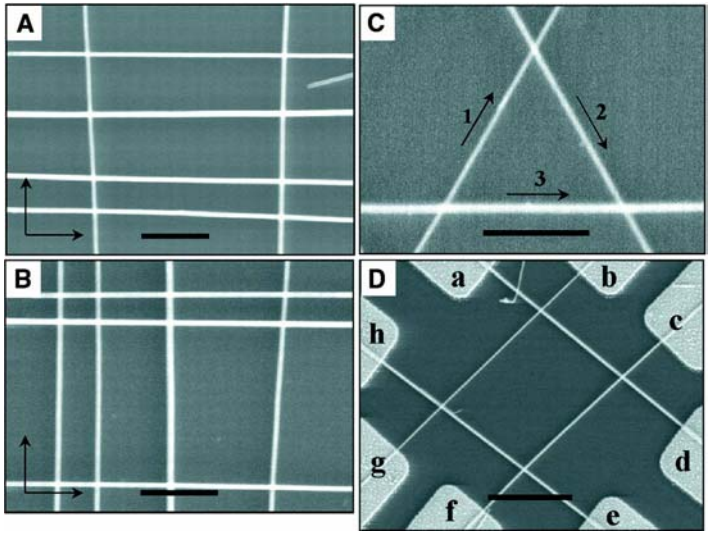
MAY require going to chemically synthesized nanostructures rather than relying on lithography

M. Radosavljevic and R. Chau, Intel Corporation

Nanotechnology Beyond 10nm Size (Beyond ~2013) – Assembly

Utilizing chemically synthesized structures will require developing chemical methods for placement, orientation and density of the structures.

E.g. fluidic assembly show by Lieber group addresses orientation issue.

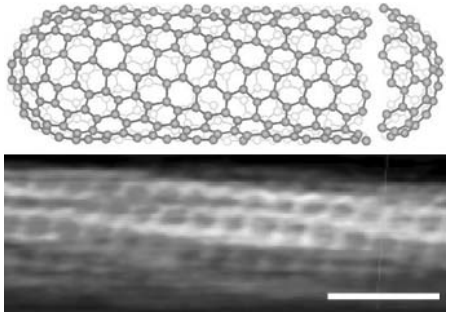


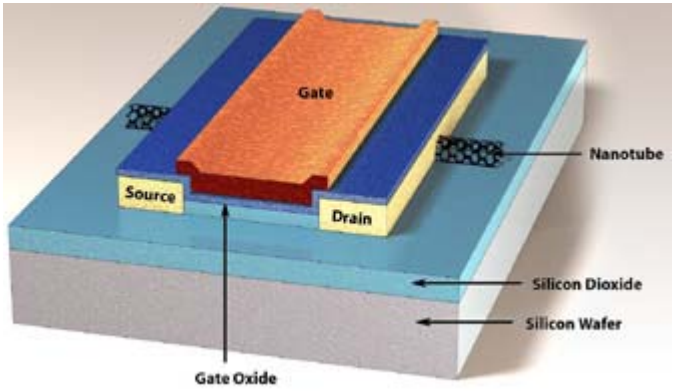
Lieber group, Science (2001).

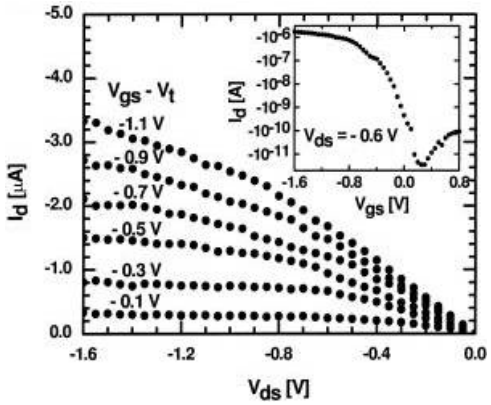
Need to establish technology that accomplish all three at the same time…
Need to find a way to deal with inherent uncertainties in these processes – defect tolerant architectures…

Nanotechnology Beyond 10nm Size (Beyond ~2013) – other materials

If chemical assembly becomes necessary why not utilize other materials with more promising performance characteristics?
E.g. Carbon nanotubes, Ge nanowires, superlattice nanowires…







IBM, Appl. Phys. Lett. (2002).

Carbon nanotubes carry as much as 10 times more current density compared to Si nanowires (similar results by Dai group at Stanford and others…)

Key Bullets

- **Silicon nanotransistors & nanotechnology will enable Moore's Law to continue through at least 2015.**
- **Electrical properties of Silicon nanotransistors still unsurpassed.**
- **Need to identify the most promising options for >2015**
  - **Must utilize Silicon technology's foundation**
  - **Semiconductor industry, academia and government need to form close collaboration**